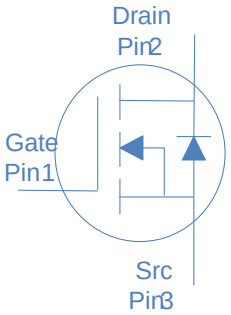
100V N-Ch Power MOSFET

Feature

- Optimized for high speed switching,Logic level
- Enhanced Body Diode dv/dt capability

V_{DS}		100	V
$R_{DS(on),typ}$	V_{GS}=10V	6.4	m :
$R_{DS(on),typ}$	V_{GS}=4.5V	7.8	m :
$I_{D\ (Sillicon\ Limited)}$		105	A
$I_{D\ (Package\ Limited)}$		70	A



Part Number	Package	Marking
HGD077N10SL	TO-252	GD077N10SL
HGI077N10SL	TO-251	GI077N10SL

Absolute Maximum Ratings at T_j

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C	105	A
		T_C	74	
Continuous Drain Current (Package Limited)		T_C	70	
Drain to Source Voltage	V_{DS}	-	100	V
Gate to Source Voltage	V_{GS}	-	±20	V
Pulsed Drain Current	I_{DM}	-	350	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.3mH, T_C	240	mJ
Power Dissipation	P_D	T_C	150	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to 175	

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Case	$R_{\theta JC}$	1	:
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	46	:

Electrical Characteristics at T_j XQOHVV RWKHUZLVH VSHFLILHG

Static Characteristics

Parameter	Symbol	Conditions	Value min	Value typ	Value max	Unit
	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250 PA	100	-		GateltSaksag CD-6(u V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250 PA	1.4	1.9	2.4	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=100V, T_j	-	-		PA
		V_{GS}=0V, V_{DS}=100V, T_j	-	-	100	
			-	-	±100	
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=20A	-	6.4		m :
		V_{GS}=4.5V, I_D=20A	-	7.8	10.0	
		V_{DS}=5V, I_D=20A	-			S
				3350	-	
			-			
			-	15		
		V_{DD}=50V, I_D=20A, V_{GS}=10V, R_G=10 : ,				

Fig 1. Typical Output Characteristics

Figure 2. On-Resistance vs. Gate-Source Voltage

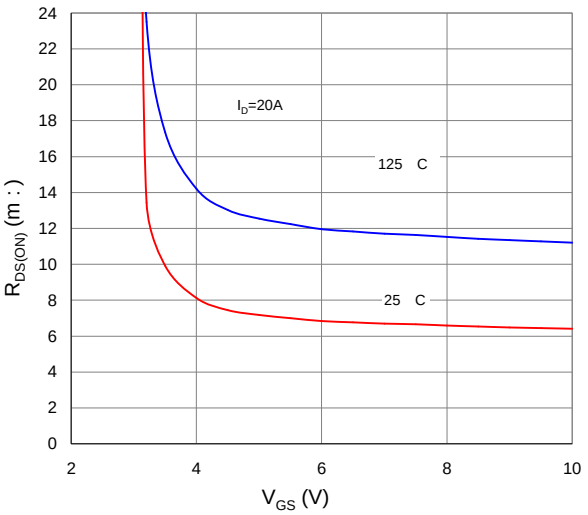
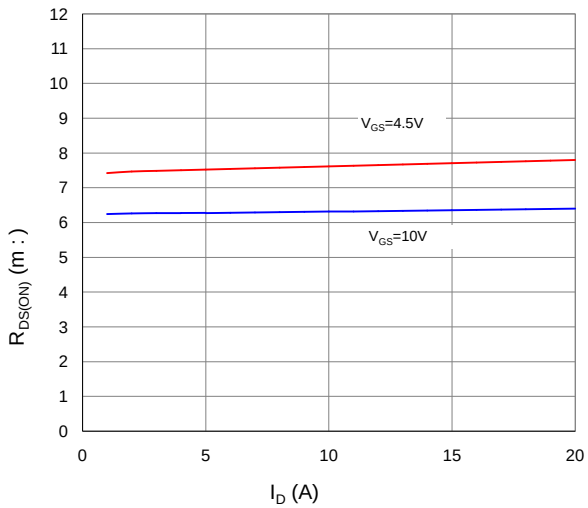


Figure 3. On-Resistance vs. Drain Current and Gate Voltage



) L J X U H 1 R U P D O L] H G 2 Q 5 H V L V W D Q F H Y V - X Q F W L R

) L J X U H 7 \ S L F D O 7 U D Q V I H U & K D U D F W H U L V W L F V

Figure 4. Typical Source-Drain Diode Forward Voltage

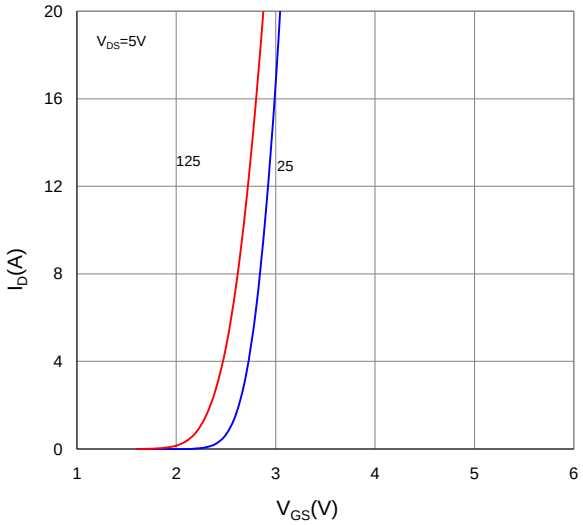


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

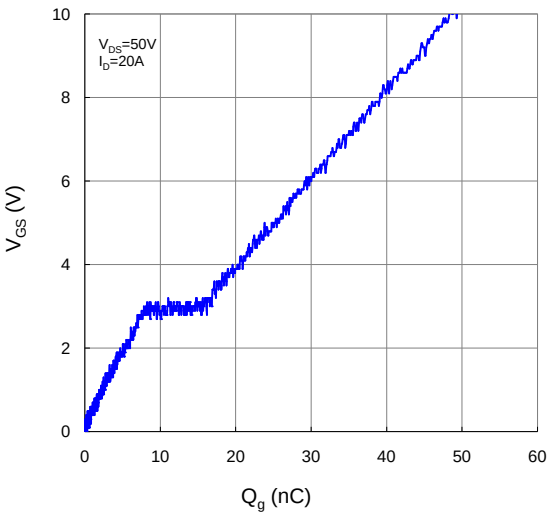
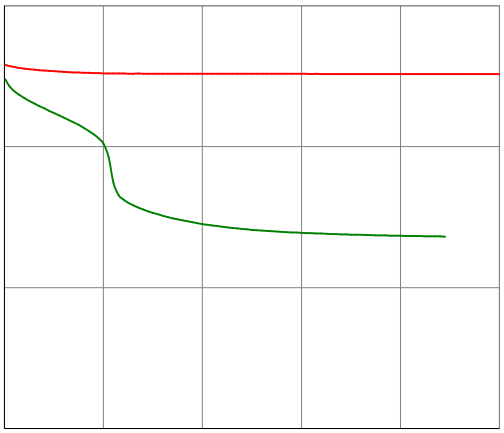


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage



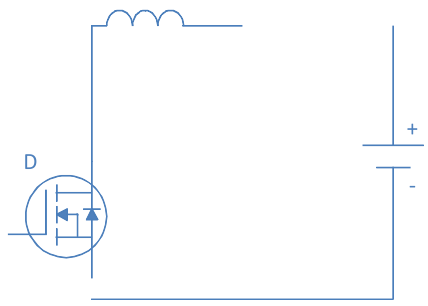
)LJXUH 0D[LPXP 6DIH 2SHUDWLQJ $UHD

Figure 10. Maximun Drain Current vs. Case Temperature

)LJXUH 1RUPDOL]HG 0D[LPXP 7UDQVLHQW 7KHUPDO ,PSHGDQFH -XQFWLR

Inductive switching Test	

Gate Charge Test	

Uclamped Inductive Switching (UIS) Test	
	

Diode Recovery Test	

Package Outline

TO-252 2 leads

TO-251, 3 leads